



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

[Handwritten signature]

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/670,911	09/28/2000	Sherry Solden	21891.03200	7789
7590	06/03/2005		EXAMINER	
John W Carpenter Crosby Heafey Roach & May P O Box 7936 San Francisco, CA 94120-7936			CRAIG, DWIN M	
			ART UNIT	PAPER NUMBER
			2123	

DATE MAILED: 06/03/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	09/670,911	SOLDEN ET AL.
	Examiner	Art Unit
	Dwin M Craig	2123

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) Responsive to communication(s) filed on 27 December 2004.
- 2a) This action is **FINAL**. 2b) This action is non-final.
- 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) Claim(s) 1-28 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) Claim(s) _____ is/are allowed.
- 6) Claim(s) 1-28 is/are rejected.
- 7) Claim(s) 29-40 is/are objected to.
- 8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) The specification is objected to by the Examiner.
- 10) The drawing(s) filed on 28 September 2000 is/are: a) accepted or b) objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
 - a) All b) Some * c) None of:
 1. Certified copies of the priority documents have been received.
 2. Certified copies of the priority documents have been received in Application No. _____.
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)	4) <input type="checkbox"/> Interview Summary (PTO-413)
2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)	Paper No(s)/Mail Date. _____.
3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.	5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)
	6) <input type="checkbox"/> Other: _____.

DETAILED ACTION

1. **Claims 1-28** have been presented for reconsideration in view of Applicants' arguments and amended claim language. New **Claims 29-40** have been presented for Examination.

Response to Arguments

2. Applicants' arguments from the 12/27/2004 response have been fully considered. The Examiner's response is as follows.

2.1 Regarding the Applicants' response to the 35 U.S.C. 112 second paragraph rejection of Claim 4.

The Examiner thanks the Applicant for the amending the rejected claim and withdraws the 35 U.S.C. 112 rejection of Claim 4.

2.2 Regarding the Applicants' response to the 35 U.S.C. 103(a) rejections of independent Claim 1.

Applicant argued, (*page 12 of the 12/27/2004 response*)

Accordingly, Pauna's determining of timing and behavior violations is entirely different from Applicant's capture of behaviors.

The Examiner relied on the *Testa et al.* reference to teach the limitation of capturing behaviors. In response to applicants' arguments against the references individually, one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.*, 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986).

2.3 Regarding the Applicants' response to the Independent Claim 1.

Applicant argued, (*pages 12 and 13 of the 12/27/2004 response*)

More importantly, Applicant's respectfully note that the examples provided by Pauna at Col. 8 lines 26-45 relate to the setting low level non-architectural parameters (e.g. setting clock speeds,), or items for debugging (e.g. notifications of register changes), etc, for Pauna's cycle accurate simulator. Therefore, the described interface is used to set up the simulator with correct clock speeds and other parameters, but does not provide mapping of captured behaviors to architectural components.

The Examiner respectfully submits that the Applicants have not specified any "special definition" as to what defines an *Architectural parameter*. The Examiner respectfully asserts that "clock speeds" are parameters that are very significant in a logic architecture. Further, and as argued in section 2.2 of this action, the Examiner relied on the *Testa et al.* reference to teach the limitation of capturing behaviors. In response to applicants' arguments against the references individually, one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.*, 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986).

2.4 Regarding the Applicant's response to the Independent Claim 1.

Applicant argued, (*page 14 of the 12/27/2004 response*).

In particular, Applicants respectfully note the above discussion related to Pauna, and specifically that which relates to Pauna's interface to the cycle accurate simulator., which cannot be equated to Applicants claimed mapping of captured behaviors to selected architectural components for at least two reasons: 1. Because Pauna's interface sets low level details rather than architectural components; 2. Because Pauna's interface is not related to captured behaviors.

The Examiner respectfully points out that the *Testa et al.* reference was relied upon to teach the limitation of capturing behaviors. In response to applicants' arguments against the references individually, one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413,

208 USPQ 871 (CCPA 1981); *In re Merck & Co.*, 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986).

The Examiner respectfully traverses Applicant's arguments and maintains the earlier 35 U.S.C. 103(a) rejections.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

The factual inquiries set forth in *Graham v. John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

3. **Claims 1-3, 6-11, 12-26** are rejected under 35 U.S.C. 103(a) as being unpatentable over **Pauna U.S. Patent 6,052,524** in view of **Testa et al. U.S. Patent 6,205,407**.

3.1 As regards independent **Claims 1 and 17** the *Pauna* reference discloses a method of modeling an electronic system having both hardware and software elements (**Col. 4 Lines 30-33**), capturing a plurality of behaviors that correspond to operations performed by the system

being modeled (**Col. 5 Lines 34-48**), the Examiner notes that determining timing and behavior violations is functionally equivalent to capturing a plurality of behaviors, capturing a plurality of hardware and software architectural components the plurality contained within an architectural platform (**Col. 6 Lines 26-38**), mapping each of the captured behaviors of the plurality of behaviors to a selected architectural component to perform the behavior (**Col. 8 Lines 26-45**) and mapping each of the captured behaviors of the plurality of behaviors to a selected architectural component to perform the behavior; (**Figure 3A Item 46, Figure 4A Item 70, Col. 13 Lines 59-67, Col. 14 Lines 1-8**), recognizing and capturing communications patterns (**Col. 4 Lines 57-67, Col. 5 Lines 1-3, Table 7 Col. 12, Col. 12 Lines 64-67 Col. 13 Lines 1-4**), the Examiner notes that the memory read routines simulated using the pseudo-code listed in Table 7 are functionally equivalent to recognizing and capturing communications patterns, specifically and in this case, the communications pattern of a processor reading from memory, among the architectural components that require communication among them to perform the behaviors (**Figure 2 Items 22 and 24, 26 and 34**), the Examiner notes that the Pauna reference is directed towards the cycle accurate simulation of the communications between different components in a system on a chip or SOC (**Col. 3 Lines 20-34**).

However, the Pauna reference does not clearly disclose, *mapping each instance of communications between behaviors to an instance of the capture pattern*.

An artisan of ordinary skill, in the SOC simulation art, would have known that in order to test the memory component in an SOC design, that certain test patterns would have to be generated and verified in order to determine if the simulated memory component was *behaving* properly. In the related art of testing ASICs, the *Testa et al.* reference discloses *mapping each*

*instance of communications between behaviors to an instance of the capture pattern (C*figure 5
Items 67, 64, all of Figures 6 & 7, Col. 7 Lines 30-52, Col. 12 Lines 5-14).

Thus, it would have been obvious, to one of ordinary skill in the art, at the time the invention was made, to have combined the component modeling methods of the *Pauna* reference with the test pattern generation methods of the *Testa et al.* reference because, in order to properly simulate and test an SOC design there is a need to generate and verify test pattern data that simulates the interaction between the components in the SOC being designed in order to verify that these components will interact correctly in the final design (*Testa et al.* Col. 2 Lines 28-33).

3.2 As regards dependent **Claims 2 and 18** the *Pauna* reference discloses components having a plurality of services corresponding to a particular function of the hardware component (**Col. 3 Lines 35-49, Col. 4 Lines 50-67, Col. 5 Lines 1-3**).

3.3 As regards dependent **Claims 3** the *Pauna* reference discloses and API (**Col. 5 Lines 4-13**).

3.4 As regards dependent **Claims 6 and 22** the *Pauna* reference discloses hardware and software (**Col. 4 Lines 30-33**).

3.5 As regards dependent **Claim 7** the *Pauna* reference discloses a plurality of services, *API* (**Col. 5 Lines 4-13**).

3.6 As regards dependent **Claims 8, 9, 10, 12, 24, 25 and 26** the *Pauna* reference does expressly discloses a history of test patterns (**Col. 8 Lines 26-45**).

3.7 As regards dependent **Claims 13 and 14** the *Pauna* reference discloses reuse of models (**Col. 4 Lines 57-67 Col. 5 Lines 1-3, Col. 8 Lines 26-45**).

3.8 As regards dependent **Claims 15, 16 and 23** the *Pauna* reference discloses a method for adding new architectures and changing the existing design from a library of components (**Col. 18 Lines 61-67 Col. 19 Lines 1-17**).

4. Independent **Claim 27** and dependent **Claims 5, 11 and 28** are rejected under 35 U.S.C. 103(a) as being unpatentable over **Pauna U.S. Patent 6,052,524** in view of **Testa et al. U.S. Patent 6,205,407** and in further view of **Hill et al. U.S. Patent 6,438,514**.

4.1 As regards the rejections of Independent **Claims 1 and 17, from which dependent Claims 5 and 11 depend**, please see paragraph 3.1 above.

4.2 As regards Independent **Claim 27** the *Pauna* reference discloses an API (**Col. 5 Lines 4-13**), and a plurality of hardware and software architectural components the plurality contained within an architectural platform (**Col. 6 Lines 26-38**), mapping each of the captured behaviors of the plurality of behaviors to a selected architectural component to perform the behavior (**Col. 8 Lines 26-45**) and mapping each of the captured behaviors of the plurality of behaviors to a selected architectural component to perform the behavior; (**Figure 3A Item 46, Figure 4A Item 70, Col. 13 Lines 59-67, Col. 14 Lines 1-8**), recognizing and capturing communications patterns (**Col. 4 Lines 57-67, Col. 5 Lines 1-3, Table 7 Col. 12, Col. 12 Lines 64-67 Col. 13 Lines 1-4**), *the Examiner notes that the memory read routines simulated using the pseudo-code listed in Table 7 are functionally equivalent to recognizing and capturing communications patterns, specifically and in this case, the communications pattern of a processor reading from memory*, among the architectural components that require communication among them to perform the behaviors (**Figure 2 Items 22 and 24, 26 and 34**),

the Examiner notes that the Pauna reference is directed towards the cycle accurate simulation of the communications between different components in a system on a chip or SOC (Col. 3 Lines 20-34).

However, the *Pauna* reference does not clearly disclose, *the first service being among a plurality of service supported by the pattern to which communication is mapped*, and a performance model of a component.

An artisan of ordinary skill, in the SOC simulation art, would have known that in order to test the memory component in an SOC design, that certain test patterns would have to be generated and verified in order to determine if the simulated memory component was *behaving* properly. In the related art of testing ASICs, the *Testa et al.* reference discloses *mapping each instance of communications between behaviors to an instance of the capture pattern* (Figure 5 Items 67, 64, all of Figures 6 & 7, Col. 7 Lines 30-52, Col. 12 Lines 5-14).

Thus, it would have been obvious, to one of ordinary skill in the art, at the time the invention was made, to have combined the component modeling methods of the *Pauna* reference with the test pattern generation methods of the *Testa et al.* reference because, in order to properly simulate and test an SOC design there is a need to generate and verify test pattern data that simulates the interaction between the components in the SOC being designed in order to verify that these components will interact correctly in the final design (*Testa et al.* Col. 2 Lines 28-33).

Hill et al. discloses a performance model (Col. 2 Lines 40-60).

It would have been obvious, to one of ordinary skill in the art, at the time the invention was made, to provide a performance model of a component because by doing so comparison of

different combinations of components could be performed without the high cost of actually fabricating the SOC (**Hill et al. Col. 2 Lines 61-64**).

4.3 As regards dependent **Claim 28** the *Pauna* reference discloses three or more components (**Figure 2 Items 22, 24, 26, 34, 30 & 32**) and it would be obvious that each of these components would have multiple services to reflect their full functionality.

4.4 As regards dependent **Claims 5 and 11** the *Pauna* reference does not expressly disclose a performance model.

The *Hill et al.* reference discloses a performance model (**Col. 2 Lines 40-60**).

It would have been obvious, to one of ordinary skill in the art, at the time the invention was made, to provide a performance model of a component because by doing so comparison of different combinations of components could be performed without the high cost of actually fabricating the SOC (**Hill et al. Col. 2 Lines 61-64**).

Allowable Subject Matter

5. **Claims 29-40** are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

6. **Claims 1- 28** have been presented for reconsideration based on Applicant's arguments and amended claim language. **Claims 29-40** have been presented for Examination. **Claims 1-28** are rejected. **Claims 29-40** are objected to.

6.1 The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Rostoker et al. **U.S. Patent 5,544,067** discloses method of simulation of behavioral architectures for logic designs.

Gregory et al. **U.S. Patent 6,132,109** discloses method of modeling logic architectures in hardware description languages.

6.2 THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

6.3 Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dwin M Craig whose telephone number is (571) 272-3710. The examiner can normally be reached on 10:00 - 6:00 M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Leo P Picard can be reached on (571)272-3749. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

DMC



**SAMUEL BRODA, ESQ.
PRIMARY EXAMINER**